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SUBJECT CODE NO: BNP-2698
FACULTY OF SCIENCE AND TECHNOLOGY
B.Sc. (NEP) (P-2024) S.Y Sem III
Examination November / December 2025
Electronics (Digital Electronics-II)

[Time: 1:00 Hours]**[Max. Marks:30]**

N. B

Please check whether you have got the right question paper.

- 1) Q.no 1 is multiple choice and it is compulsory.it carries 10 marks.
- 2) Attempt any four question from Q.no 2 to Q.no 7 each of these question carries 5 mark
- 3) Figure to right indicate full marks

PART-A**Q1 Attempt all MCQ****10**

1. When RESET is the enable in SR Flip-flop_____
 - A) SET B) RESET C) preset D) NO-change.
2. How many Flip-Flops are required to design 4-bit ring counter.
 - A) 2 B) 3 C) 4 D) 5
3. 3) A decade counter counts from 0 to _____
 - A) 9 B) 5 C) 7 D) 15
4. Which shift register allows inputs bits to be entered simultaneously in all stages.
 - A) SISO B) SIPO C) PIPO D) None of the above.
5. _____ are the applications of Flip-Flop.
 - A) Register B) counters C) storage device D) All of the above

PART-B

- | | |
|---|-----------|
| Q2 Explain S-R Flip-Flop | 05 |
| Q3 Explain 3-bit asynchronous counter | 05 |
| Q4 Explain Ring counter | 05 |
| Q5 Explain D-Flip-flop. | 05 |
| Q6 Explain serial in serial out shift register | 05 |
| Q7 Explain Buffer register. | 05 |