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SUBJECT CODE NO:- B-2146
FACULTY OF SCIENCE & TECHNOLOGY
B.Sc. T. Y. (Sem-V)
Examination November/December- 2022
Electronics Paper- XVI
8085 Interfacing-I

[Time: 1:30 Hours]

[Max. Marks: 50]

“Please check whether you have got the right question paper.”

- N.B
- i) Attempt all questions.
 - ii) Illustrate your answer with suitable labeled diagram.
- Q. 1 Explain use of decoder for chip select logic. Give the procedural steps and logic design to interface 2K byte of memory to 8085 microprocessor with starting address 8000H using 3 : 8 decoder. 20
- OR
- Enlist any five features of 8255 PPI. Draw the block diagram of 8255 PPI and explain function of each block in detail. 20
- Q. 2 Write any five features of 8251 USART. Draw the block diagram of 8251 USART and write use of signals associated with each block. 20
- OR
- Write short notes (any four) 20
- a) Procedure and logic diagram to demultiplex address and data bus in 8085 microprocessor.
 - b) Working of mode 1 of 8255 PPI
 - c) Transmission section of 8251 USART
 - d) Read / Write control logic in 8255 USART.
 - e) I/O mode control word format of 8255 PPI
 - f) Generation of memory & I/O read/write signals in 8085 microprocessor.
- Q. 3 Attempt the following by selecting correct answer. 10
- 1) BSR mode of 8255 PPI is for _____.
 - (a) Port A
 - (b) Port B
 - (c) Port C
 - (d) Port A and Port B

- 2) ALE signal is used to latch _____.
 - (a) Data
 - (b) lower byte of address
 - (c) higher byte of address
 - (d) lower & higher bytes of address

- 3) \overline{CS} pin of the device is used for _____.
 - (a) to read data
 - (b) Write data
 - (c) Select device for read / write
 - (d) none of the above

- 4) Number of I/O modes of 8255PPI are _____.
 - (a) 3
 - (b) 4
 - (c) 6
 - (d) 8

- 5) In mode 1 of 8255, the strobe bits for Port A are provided by _____.
 - (a) Port B lower
 - (b) Port B upper
 - (c) Port C lower
 - (d) Port C upper

- 6) The internal bus of 8251 USART is of _____ bit.
 - (a) 4
 - (b) 6
 - (c) 8
 - (d) 10

- 7) _____ Signal is for modem control block of 8251 USART.
 - (a) \overline{RTS}
 - (b) RxD
 - (c) \overline{RxC}
 - (d) \overline{RD}

- 8) _____ signal is for Read / Write control block of 8251 USART.
 - (a) \overline{DTR}
 - (b) \overline{DSR}
 - (c) \overline{WR}
 - (d) TxD

- 9) 3 : 8 demultiplexer has _____ input data lines.
- (a) 1
 - (b) 2
 - (c) 4
 - (d) 8
- 10) For selection to control word register in 8255 PPI, the address line A_1A_0 should be _____.
- (a) 00
 - (b) 01
 - (c) 10
 - (d) 11