Total No. of Printed Pages:2

SUBJECT CODE NO:- 2173
FACULTY OF SCIENCE AND TECHNOLOGY
B.Sc. T.Y Sem. VI
Examination March/April-2022 (To Be Held In June/July-2022)
B) 8085 Interfacing-II

[Time: 1:53 Hours] **[Max. Marks: 50]**

Please check whether you have got the right question paper.

N.B 1) Attempt all questions
2) Illustrate yours answer with suitable labeled diagram

Q.1 a) Explain the functional block diagram of the 8253 /8254 10

b) What is DMA controller? Explain with the block diagram 10

OR

a) Describe the TRAP & RST 7.5 , 6.5 & 5.5 10

b) Explain DMA operation 10

Q.2 Explain programmable interrupt controller 8259 with schematic diagram 20

OR

Write a short notes on any four 20

a) Resistor organization of the OTC 8259
b) Signal PIC system and cascaded PIC's system
c) Mode set resister & status resister
d) Basic DMA definition
e) Control word resister format of 8253/8254
f) Pin Configurations of the 8255/8254

Q.3 Attempt the following multiple choice questions 10

1) -------- is memory write
a) MEMW b) MEMR c) HRG d) none of these
2) These are DMA acknowledge lines
a) $A_o - A_7$ b) $DRQ_o - DRQ_3$ c) $DACK_6 - DACK_3$ d) none of these

3) 8254 provide a -----source to the interval speaker & other devices
   a) $18.5H_3$ b) $18.2H_4$ c) $50.2H_4$ d) $82.6H_4$
4) 8253 uses NMOS technology where as 8254 uses
   a) HMOS b) PMOs c) both a & b d) none of these
5) Read A low on this pin enables 8259 to send various status signals on the data bus for CPU
   a) $\overline{wR}$ b) $\overline{CS}$ c) $\overline{RD}$ d) none of these
6) Interrupt requests I?O devices send interrupt request through there lines
   a) $IR_O - IR_7$ b) $IR_7 - IR_o$ c) IR d) none of these
7) The program sequence is transferred to the memory location specified by ---- instruction
   a) Out b) In c) CALL d) Input
8) The counter start counting after the rising edge of the trigger input output low for one clock period when the termined count is
   a) Reabled b) unrenched c) stable d) unstable
9) MODEz is called eisher rate generator or divide by
   a) (N-1) counter b) N counter c) (N+1) counter d) none of these
10) I/O read it is a bidirectional line in output mode it is used to access data from she I/O device during she DMA read cycle
   a) $\overline{I/OR}$ b) I/ow c) TC d) I/o