## **Examination October 2020**

B.Sc. F.Y (Sem-I)

## 2178 Computer Science Paper-II CS02 Digital Electronics

Max. Marks: 25

Time: One Hour

Instructions

Solve any 25 questions from Q.1 to Q.30

1 The number 1001012 is equivalent to	Decimal			
(A)54	(B)45	(C)37	(D)25	
2 Convert binary 111111110010 to he:				
(A)EE216	(B)FF216	(C)2FE16	( <b>D</b> )FD216	
3 An important drawback of binary sys		(0)21110		
1 0 0	d (B)It requires sparingly small string of 1's	(C) It requires large string of 1's and small	(D) It requires small string of 1's and large	
0's to represent a decimal number	and 0's to represent a decimal number		string of 0's to represent a decimal number	
4 Convert the hexadecimal number (11	E2)16 to decimal:			
(A)480	(B)483	(C)482	(D)484	
5 Binary subtraction of 101101 – 0010	11 = ?			
(A)100010	(B)010110	(C)110101	(D)101100	
6 2's complement of 11001011 is				
(A)01010111	(B)11010100	(C)00110101	(D)11100010	
7 The involution of A is equal to				
(A)A	(B)A'	(C)1	(D)0	
8 The logical sum of two or more logic	cal product terms is called			
(A)SOP	(B)POS	(C)OR operation	(D)NAND operation	
9 There are Minterms				
(A)0	(B)2	(C)8	(D)1	
	design and therefore are a			
(A)Sampling	(B)Digital	(C)Analog	(D)Systems	
11 The output of an EX-NOR gate is 1.		(-)	(_)_)	
(A)A = 1, B = 0	(B)A = 0, B = 1	(C)A = 0, B = 0	(D)A = 0, B' = 1	
12 The number of full and half adders a		(0), 2 0		
(A)8 half adders, 8 full adders	(B)1 half adders, 15 full adders	(C)16 half adders, 0 full adders	(D)4 half adders, 12 full adders	
(A)s hair adders, 8 run adders (D)4 hair adders, 12 run adders (C)16 hair adders, 0 run adders (D)4 hair adders, 12 run adders 13 A universal logic gate is one which can be used to generate any logic function. Which of the following is a universal logic gate?				
1.3 A universal logic gate is one which a	an be used to generate any logic function. W	hich of the following is a universal logic ga	ite?	
(A)OR	(B)AND	hich of the following is a universal logic ga (C)XOR	(D)NAND	
(A)OR 14 A full adder logic circuit will have _	(B)AND	(C)XOR	(D)NAND	
<ul><li>(A)OR</li><li>14 A full adder logic circuit will have _</li><li>(A)Two inputs and one output</li></ul>	(B)AND (B)Three inputs and three outputs			
<ul> <li>(A)OR</li> <li>14 A full adder logic circuit will have</li> <li>(A)Two inputs and one output</li> <li>15 Why XOR gate is called an inverter?</li> </ul>	(B)AND (B)Three inputs and three outputs	(C)XOR (C)Two inputs and two outputs	(D)NAND (D)Three inputs and two outputs	
<ul> <li>(A)OR</li> <li>14 A full adder logic circuit will have</li> <li>(A)Two inputs and one output</li> <li>15 Why XOR gate is called an inverter</li> <li>(A)Because of the same input</li> </ul>	(B)AND (B)Three inputs and three outputs (B)Because of the same output	<ul><li>(C)XOR</li><li>(C)Two inputs and two outputs</li><li>(C)It behaves like a NOT gate</li></ul>	(D)NAND	
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## **Examination October 2020**

(A)1	(B)2	(C)3	(D)4	
25 The number of input variable which a NOT gate can have is				
(A)One	(B)Two	(C)Three	(D)Any Number	
26 Under What condition the Output of two input AND gate is One				
(A)Both the inputs are 0	(B)Any one input is 0	(C)Both the inputs are 1	(D)Both the inputs are 0	
27 What are the number of digits of hexadecimal number system				
(A)2	(B)4	(C)8	(D)16	
28 Data can be changed from special code to temporal code by using				
(A)Shift registers	(B)counters	(C)Combinational circuits	(D)A/D converters	
29 The gates required to build a half adder are				
(A)EX-OR gate and NOR gate	(B)EX-OR gate and OR gate	(C)EX-OR gate and AND gate	(D)Four NAND gates	
30 DeMorgan's first theorem shows the equivalence of				
(A)OR gate and Exclusive OR gate	(B)NOR gate and Bubbled AND gate	(C)NOR gate and NAND gate	(D)NAND gate and NOT gate	