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Examination October 2020

B.Sc. F.Y (Sem-I)

2178 Computer Science Paper-II CS02 Digital Electronics

Time: One Hour **Max. Marks: 25**

Instructions

Solve any 25 questions from Q.1 to Q.30

1 The number 1001012 is equivalent to Decimal

(A)54 (B)45 (C)37 (D)25

2 Convert binary 111111110010 to hexadecimal.

(A)EE216 (B)FF216 (C)2FE16 (D)FD216

3 An important drawback of binary system is _____

(A)It requires very large string of 1's and 0's to represent a decimal number (B)It requires sparingly small string of 1's and 0's to represent a decimal number (C)It requires large string of 1's and small string of 0's to represent a decimal number (D)It requires small string of 1's and large string of 0's to represent a decimal number

4 Convert the hexadecimal number (1E2)16 to decimal:

(A)480 (B)483 (C)482 (D)484

5 Binary subtraction of 101101 – 001011 = ?

(A)100010 (B)010110 (C)110101 (D)101100

6 2's complement of 11001011 is _____

(A)01010111 (B)11010100 (C)00110101 (D)11100010

7 The involution of A is equal to _____

(A)A (B)A' (C)1 (D)0

8 The logical sum of two or more logical product terms is called

(A)SOP (B)POS (C)OR operation (D)NAND operation

9 There are _____ Minterms for 3 variables (a, b, c).

(A)0 (B)2 (C)8 (D)1

10 These logic gates are widely used in _____ design and therefore are available in IC form.

(A)Sampling (B)Digital (C)Analog (D)Systems

11 The output of an EX-NOR gate is 1. Which input combination is correct?

(A)A = 1, B = 0 (B)A = 0, B = 1 (C)A = 0, B = 0 (D)A = 0, B' = 1

12 The number of full and half adders are required to add 16-bit number is

(A)8 half adders, 8 full adders (B)1 half adders, 15 full adders (C)16 half adders, 0 full adders (D)4 half adders, 12 full adders

13 A universal logic gate is one which can be used to generate any logic function. Which of the following is a universal logic gate?

(A)OR (B)AND (C)XOR (D)NAND

14 A full adder logic circuit will have _____

(A)Two inputs and one output (B)Three inputs and three outputs (C)Two inputs and two outputs (D)Three inputs and two outputs

15 Why XOR gate is called an inverter?

(A)Because of the same input (B)Because of the same output (C)It behaves like a NOT gate (D)It behaves like a AND gate

16 A logic circuit that provides a HIGH output for both inputs HIGH or both inputs LOW is _____

(A)Ex-NOR gate (B)OR gate (C)Ex-OR gate (D)NAND gate

17 Latch is a device with _____

(A)One stable state (B)Two stable state (C)Three stable state (D)Infinite stable states

18 Which of the following is correct for a gated D-type flip-flop?

(A)The Q output is either SET or RESET as soon as the D input goes HIGH or LOW (B)The output complement follows the input when enabled (C)Only one of the inputs can be HIGH at a time (D)The output toggles if one of the inputs is held HIGH

19 A basic S-R flip-flop can be constructed by cross-coupling of which basic logic gates?

(A)AND or OR gates (B)XOR or XNOR gates (C)NOR or NAND gates (D)AND or NOR gates

20 The output of a JK flipflop with asynchronous preset and clear inputs is '1'. The output can be changed to '0' with one of the following conditions.

(A)By applying J = 0, K = 0 and using a clock (B)By applying J = 1, K = 0 and using the clock (C)By applying J = 1, K = 1 and using the clock (D)By applying a synchronous preset input

21 How many flip-flops are required to construct a register which is capable of storing 409610 in binary

(A)8 (B)10 (C)12 (D)14

22 A counter that counts from 0 to 7 is called

(A)mod – 8 counter (B)mod -7 counter (C)mod – 10 counter (D)mod – 6 counter

23 What will be the maximum number of flips flops are required for a mod – 9 counter

(A)9 flip-flops (B)18 flip-flops (C)3 flip-flops (D)4-flip-flops

24 The number of control lines required for a 1 to 8 multiplexer will be

(A)1 (B)2 (C)3 (D)4

25 The number of input variable which a NOT gate can have is

(A)One (B)Two (C)Three (D)Any Number

26 Under What condition the Output of two input AND gate is One

(A)Both the inputs are 0 (B)Any one input is 0 (C)Both the inputs are 1 (D)Both the inputs are 0

27 What are the number of digits of hexadecimal number system

(A)2 (B)4 (C)8 (D)16

28 Data can be changed from special code to temporal code by using

(A)Shift registers (B)counters (C)Combinational circuits (D)A/D converters

29 The gates required to build a half adder are

(A)EX-OR gate and NOR gate (B)EX-OR gate and OR gate (C)EX-OR gate and AND gate (D)Four NAND gates

30 DeMorgan’s first theorem shows the equivalence of

(A)OR gate and Exclusive OR gate (B)NOR gate and Bubbled AND gate (C)NOR gate and NAND gate (D)NAND gate and NOT gate