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Examination October 2020

B.Sc. T.Y (Sem-VI)

2068B Electronics Paper- XX (602) B) 8085 Interfacing-II

Time: One Hour **Max. Marks: 25**

instruction

- solve any 25 questions from Q.1 to Q.30

1 The number of counters that are present in the programmable timer device 8254 is

(A) 1 (B) 2 (C) 3 (D) 4

2 In mode 2, if N is loaded as the count value, then after (N-1) cycles, the output becomes low for

(A) 1 clock cycle (B) 2 clock cycles (C) 3 clock cycles (D) 4 clock cycles

3 In control word format, if RL1=1, RL0=1 then the operation performed is

(A) read/load least significant byte only (B) read/load most significant byte only (C) read/load LSB first and then MSB (D) read/load MSB first and then LSB

4 The programmable timer device (8253) contains three independent _____ bit counters.

(A) 8 (B) 16 (C) 20 (D) 32

5 The specialty of the 8253 counters is that they can be easily read on line without disturbing the _____ input to the counter.

(A) GATE (B) CLK (C) OUT (D) WR

6 In control word format, if RL1=1, RL0=1 then the operation performed is

(A) read/load least significant byte only (B) read/load most significant byte only (C) read/load LSB first and then MSB (D) read/load MSB first and then LSB

7 If the count loaded is odd the first clock cycle pulse decrement by _____ resulting in an even count value.

(A) 0 (B) 1 (C) -1 (D) None of these

8 In control word register format counter 1 is selected when D7 is____ and D6 is _____

(A) 0,0 (B) 0,1 (C) 1,0 (D) 1,1

9 When RL1 is 0 and RL2 is 1, which operation is selected

(A) Counter Latching Operation (B) Read/ Load LSB only (C) Read/ Load MSB only (D) Read/ Load LSB first and then MSB

10 In control word register format counter 0 is selected when SC1 is____ and SC0 is _____

(A) 0,0 (B) 0,1 (C) 1,0 (D) 1,1

11 In direct memory access mode, the data transfer takes place

(A) directly (B) indirectly (C) directly and indirectly (D) none of the mentioned

12 In 8257 register format, the selected channel is disabled after the terminal count condition is reached when

(A) Auto load is set (B) Auto load is reset (C) TC STOP bit is reset (D) TC STOP bit is set

13 The pin that disables all the DMA channels by clearing the mode registers is

(A) MARK (B) CLEAR (C) RESET (D) READY

14 The pin that strobes the higher byte of the memory address, generated by the DMA controller into the latches is

(A) AEN (B) ADSTB (C) TC (D) None of the mentioned

15 In control word register format counter 1 is selected when D7 is____ and D6 is _____

(A) 0,0 (B) 0,1 (C) 1,0 (D) 1,1

16 The number of clock cycles required for an 8257 to complete a transfer is

(A) 2 (B) 4 (C) 8 (D) none of the mentioned

17 The register of 8257 that can only be written in is

(A) DMA address register (B) Terminal count register (C) Mode set register (D) Status register

18 The DMA differs from the interrupt mode by

(A) The involvement of the processor for the operation (B) The method accessing the I/O devices (C) The amount of data transfer possible (D) Both a and c

19 The DMA controller has _____ registers

(A) 4 (B) 3 (C) 2 (D) 1

20 The technique where the controller is given complete access to main memory is

(A) Cycle stealing (B) Memory stealing (C) Memory Con (D) Burst mode

21 The number of hardware interrupts that the processor 8085 consists of is

(A) 1 (B) 3 (C) 5 (D) 7

22 The interrupt control logic

(A) manages interrupts (B) manages interrupt acknowledge signals (C) accepts interrupt acknowledge signal (D) all of the mentioned

23 Once the ICW1 is loaded, then the initialization procedure involves

(A) edge sense circuit is reset (B) IMR is cleared (C) slave mode address is set to 7 (D) all of the mentioned

24 The pin that strobes the higher byte of the memory address, generated by the DMA controller into the latches is

(A) AEN (B) ADSTB (C) TC (D) None of the mentioned

25 8259 manage ___ interrupt requests

(A) 2 (B) 4 (C) 6 (D) 8

26 To write command word into ICW1 register A0 pin should be at logic____

(A) 0 (B) 1 (C) 2 (D) -1

27 If ADI = 1 gives spacing between two successive ISR will be ____ bytes

(A) 4 (B) 6 (C) 16 (D) 64

28 _____ command is used to program higher byte of ISR address in 8085 mode

(A) ICW1 (B) ICW2 (C) ICW3 (D) ICW4

29 fully nested mode when SFNM=____

(A) 0 (B) 1 (C) 2 (D) -1

30 For reset special mask ESMM=_____ and SMM= _____

(A) 0,0 (B) 0,1 (C) 1,0 (D) 1,1