B-2212

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SUBJECT CODE NO:- B-2212
FACULTY OF SCIENCE AND TECHNOLOGY
B.Sc. S.Y (Sem.-IV) Examination OCT/NOV 2019
Electronics Paper- XII
A) 8086 Microprocessor Interfacing

[Time: 1:30 Hours] **[Max.Marks:50]**

Please check whether you have got the right question paper.

N.B
1) Attempt all questions.
2) Illustrate your answer with suitable labelled diagram.

Q.1 Draw the pin diagram of 8255 PPI and function of each pin. Explain the modes of 8255. 20

OR

Design an interface of input port 74LS245 to read the status of 8 switches and display the status on 8 LED's using output port 74LS373 and write an ALP. 20

Q.2 Draw the Architecture of 8253 and explain each block in detail. 20

OR

Write short note on any four of the followings. 20

1) DRAM interfacing
2) Methods of data communication
3) BSR mode of 8255
4) DAC Interfacing
5) Command word of 8251
6) Write an ALP for 8 switches interfacing

Q.3 Multiple choice questions 10

1) In mode "0" of 8255 Can_____
   a) Any port can use as I/O b) Output ports are latched
   c) Input ports are buffered d) All of the above

2) Eoc stands for_____
   a) End of conversion b) End of controller c) End of code d) None of these

3) 8255 consist _____ no of I/O lines
   a) 24 b) 20 c) 16 d) 20

4) _____pin is used in 8251 to control rate of character transmission.
   a) $\overline{T \times C}$ b) $\overline{T \times D}$ c) $R \times C$ d) $T \times C$

5) 74LS245 is _____
   a) Bidirectional buffer b) 8 bit input port c) 8 bit buffer d) All of the above

6) $\overline{INTA}$ is_____
   a) Interrupt Acknowledge b) Interrupt Enable
   c) Intercept Acknowledge d) Interrupt available

7) $\overline{T \times C}$ pin used in 8253 for_____
   a) Transmitter clock input b) Transmit data
   c) Transmit control signal d) Transmit data and clock

8) 8251 is _____ receiver and Transmitter.
   a) Synchronous b) Asynchronous
   c) Synchronous and Asynchronous d) None of these

9) $\overline{RD}$ pin used in 8086 up for_____
   a) Read b) Write c) Read & Write d) Enable

10) 8251 is available in _____DTP package.
   a) 28 b) 40 c) 20 d) 14

OR

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B.Sc. S.Y (Sem.-IV) Examination OCT/NOV 2019
Electronics Paper- XII
B) 8085 Microprocessor-II

[Time: 1:30 Hours] **[Max.Marks:50]**

Please check whether you have got the right question paper.

N.B
3) Attempt all questions.
4) Illustrate your answer with suitable labelled diagram.

Q.1 Explain stack & stack related instructions. 20

OR

Explain the Block diagram of 8085 microprocessor. 20

Q.2 Explain serial data transfer techniques. 20

OR

Write short notes on any four from the following each 5 marks. 20

a) Pin Definitions & diagram A1,A0, LLK, CS, G,GND out
b) Control word Resister format of 8253/8254
c) Resister organisation of 8257
d) Basic DMA definitions
e) Resister organization of the PIC 8259
f) Single PIC system & cascaded PIC's system

Q.3 Attempt the following multiple choice question by selecting correct option 10

1) 8085 microprocessor has how many ping
a) 30 b) 39 c) 40 d) 42

2) The first microprocessor to include virtual memory in the intel microprocessor family is_____

a) 80386 b) 80486 d) 80286 d) Pentium

3) The total time required to execute an instruction is_____
a) IC=FC+EC b) FC=EC+IC c) Both of a & b d) None of these

4) When the _____ is executed the stack pointer register is decremented by two.
a) PUSH b) CALL c) RET d) POP

5) The documentation should in include _____
a) Functions & the subroutine b) I/O parameters
c) All least one of the above d) None of these

6) _____of data is used for short distance.
a) Parallel transmission b) Serial transmission c) Very long distance d) All of these

7) In synchronous data transfer_____
a) Three separate clock inputs can be used. b) Two separate clock inputs can be used
c) Only one clock can be used. d) None of these

8) Devices or DMA data transfer is subdivided in_____
a) Burst or Block transfer DMA b) Cycle steal or single byte transfer DMA
c) Transparent or hidden DMA d) All of the above

9) Hardware interrupt is requested by _____
a) Internal b) External c) Both of a & b d) None of these

10) Response time of non maskable interrupts is_____
a) High b) Low c) Constant d) None of these