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**SUBJECT CODE NO: - Y-2173**  
**FACULTY OF SCIENCE AND TECHNOLOGY**  
**B.Sc. T.Y (Sem-VI)**  
**Examination March / April - 2023**  
**8085 Interfacing-II**

[Time: 1:30 Hours]

[Max. Marks: 50]

N. B

- 1) Please check whether you have got the right question paper.
- 2) Attempt all questions

Q.1 Write Four points of comparison between 8253 and 8254 programmable interval timer. 20

What is use of A0, A1 and  $\overline{CS}$  pins of 8253. Explain working of 8253 in mode 1 with the help of three cases and timing diagrams.

**OR**

Draw the labelled block diagram of 8253 programmable interval timer. Explain working of 8253 in mode 4 with the help of three cases and timing diagrams.

Q.2 Draw the flowchart of cycle steal DMA data transfer. Discuss any twelve points of comparison between slave and master mode of 8257 DMA controller. 20

**OR**

Write short notes ( any four )

- 1) Block diagram of 8259 PIC
- 2) Use and format of initialization command word ICW1
- 3) Status read operation of operational command word OCW3.
- 4) Interrupt operations in cascaded PIC5
- 5) Features of 8259 PIC
- 6) Pin diagram of 8257 DMA controller.

Q.3 Rewrite the following by selecting correct answer from given options. 10

- 1) The maximum operating frequency for 8253 programmable interval times is \_\_\_\_
  - a. 1MHz
  - b. 2MHz
  - c. 3MHz
  - d. 4MHz
- 2) Each counter of 8253 is of \_\_\_\_\_ bits.
  - a. 8
  - b. 10
  - c. 12
  - d. 16

- 3) For section of 8253, logic 0 is applied to \_\_\_\_\_ pin  
a.  $\overline{RD}$                       b. CLK 1                      c.  $\overline{CS}$                       d.  $\overline{WR}$
- 4) \_\_\_\_\_ is the bi – directional signal of 8253 DMA controller  
a. CLK                      b. DO                      c.  $\overline{CS}$                       d. AO
- 5) \_\_\_\_\_ is the bi-directional signal of 8553 DMA controller.  
a. HOLD                      b. HLDA                      c. AEN                      d.  $\overline{IOR}$
- 6) TC register of 8257 DMA controller is of \_\_\_\_\_ bits  
a. 8                      b. 16                      c. 32                      d. 64
- 7) The mode set register of 8257 DMA controller is \_\_\_\_\_ register.  
a. Read only                      b. Write only                      c. Read / write                      d. Note accessible
- 8) \_\_\_\_\_ signal is relaxed with control logic block of 8257 DMA controller.  
a.  $\overline{CS}$                       b. RESET                      c. HLDA                      d. CLK
- 9) The 8259 programmable interrupt controller is \_\_\_\_\_ pin IC.  
a. 20                      b. 28                      c. 32                      d. 40
- 10) \_\_\_\_\_ pin of 8259 interrupt controller is bidirectional.  
a. CAS2                      b.  $\overline{RD}$                       c. INT                      d.  $\overline{CS}$